IN THE SPECIFICATION:

Please enter the following amendments to the specification:

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As shown in FIG. 2A, a predetermined circuit pattern is formed (S1) by an etching process, etc., on an electroconductive material 2 on a board material such as a copper foil stacking board comprising a printed circuit board 1 of an insulating material and the electroconductive material 2, such as copper, as shown in FIG. 2B. In this case, in place of a copper foil stacking board, a metal such as Zn, Ni, Ag, Pd, Cr, Ti, Be, W, Rh, Ru, etc., or an alloy thereof or an oxide electrode material, such as indium oxide or ruthenium oxide, can be attached, as an electrode material, in the form of a foil, or plated, or formed by a thin film method, such as an evaporation method, on a proper substrate. Then, as shown in FIG. 2C, a dry film resist (hereinafter referred to as a DF) 3 formed of, for example, a photosensitive film, is stacked on the electroconductive material 2 (S2) and those portions other than projection electrode formation areas 4 formed on the wiring board's electrodes, serving as the portions of a circuit pattern, are masked with a mask 5 and exposed to light. After the removal of the mask 5, development is made, thus eliminating the [DF3] DF 3 (S3) other than the projection electrode formation areas 4 on the wiring board 1 as shown in FIG. 2D. FIG. 4 is a view from above, of a partially eliminated [DF3] DF 3 and wiring board 1 and, at the step S3, holes 31 are provided where the [DF3] DF 3 has been eliminated. By doing so, the DF mask portion 30 provides no isolated pattern and the problem involving peeling of the DF mask portion 30 by the etching

process can never occur. It is to be noted that FIG. 2E is a cross-sectional view taken along broken line A-A' of the wiring board 1 in FIG. 4.

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Then, as shown in FIG. 2E, the wiring board 1 is subjected to an isotropic etching process, by which the electroconductive material 2 is gradually etched at those portions other than the projection electrode formation areas 4, to provide projection electrodes 7 having pointed tapering ends in vertical cross-section (S4). If, at this time, under a wet etching process for example, overetching is effected beneath the [DF3] DF 3 through the utilization of an isotropic corrosion action, it is possible to provide projection electrodes 7 having a sharp-pointed bump end. Finally, the wiring board 1 is exposed to a DF elimination solution of, for example, a halogen-series organic solvent, to remove remaining [DF3] DF 3 from the projection electrode 7 (S5) as shown in FIG. 2F. A plating process is performed on the etched electroconductive material 2 with the use of rhodium (Rh), palladium (Pd), gold (Au), etc., to provide a plated layer 8 as shown in FIG. 2G, and thus complete the projection electrodes. Although, in the example of this projection electrode forming process, a negative type resist has been explained as the [DF3] DF 3, even if a light exposure/development process is effected at step S3 with the use of a positive type resist, it is also possible to obtain projection electrodes by an etching process, provided that, in this case, a simple reverse relation is involved between the hole 31 with the DF removed and the DF mask area 30. Further, an added corrosion resistance, etc., can be obtained by performing a plating process on the electroconductive material 2.

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FIG. 5 is a perspective view showing a wiring board 1 equipped with projection electrodes 7 having bump configurations, the projection electrode corresponding to a second embodiment of the present invention. The projection electrodes 11 formed on the wiring board 1 with the same process as set out above, are formed in a manner to be connected to a circuit pattern 10 and equipped with ridge bumps 7b having a pointed tapering end in vertical cross-section. In this embodiment, the pointed tapering end is adapted to be linearly connected to an associated electrode and ensures a positive electrical connection to the associated electrode with less connection resistance at the time of connection. It is, therefore, possible to reduce the pressing force of a semiconductor chip with which the chip is mounted. The shape of the projection electrode 11 can be freely determined by changing the process conditions of the thickness and material of the [DF3] DF 3, composition components of an etching solution or temperature, etc., for example, at the steps S2 to S4. That is, since the direction, etc., in which an electroconductive material 2 is etched with the etching solution can be controlled by changing the process conditions, it is possible to produce the projection electrode 11 having the bump 7a as shown in FIG. 5 and contacting projection electrode 21 having the bump 7a as shown in FIG. 1B to a desired shape and to achieve less variation, etc., in the shape of the projection electrode.

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In order to form such a bump 7b at the projection electrode 11, it is only necessary to

achieve masking with the [DF3] DF 3 as shown in FIG. 6. The masking by the [DF3] DF 3 is effected by forming narrower holes 32, 33 and 34 at a middle and both sides on the projection electrode 11 over the [DF3] DF 3. Bumps 7b of a regular shape, size, etc., can be easily formed beneath the DF mask portions 35, 36 between the holes 32, 33 at one side and between the holes 32 and 34 at the other side, under an isotropic corrosion action of an etching solution from the hole portions 32, 33 and 34. Even in this case, the DF mask portions 35 and 36 stays in a not-isolated pattern. Further, according to the formation method of the projection electrode, the respective bumps are not so formed as to be connected by a plating or bonding, etc., method on to the wiring board's electrode and it is, therefore, possible to enhance the peeling resistance of the bump.